### MGT/FPGA CLOCK MANAGEMENT SYSTEM

Eric D. Groen
Charles W. Boecker
William C. Black
Scott A. Irwin
Joseph Neil Kryzak

#### BACKGROUND OF THE INVENTION

#### TECHNICAL FIELD OF THE INVENTION

[0001] This invention relates generally to communication systems and more particularly to clock recovery circuits used therein.

### DESCRIPTION OF RELATED ART

Communication systems are known to transport large amounts of data between a plurality of end user devices, which, for example, include telephones, facsimile machines, computers, television sets, cellular telephones, personal digital assistants, etc. As is known, such communication systems may be local area networks (LANs) and/or wide area networks (WANs) that are stand-alone communication systems or interconnected to other LANs and/or WANs as part of a public switched telephone network (PSTN), packet switched data network (PSDN), integrated service digital network (ISDN), or Internet. As is further known, communication systems include a plurality of system equipment to facilitate the transporting of data. Such system equipment includes, but is not limited to, routers, switches, bridges, gateways, protocol converters, frame relays, private branch exchanges.

[0003] The transportation of data within communication systems is governed by one or more standards that ensure the integrity of data conveyances and fairness of access for data conveyances. For example, there are a variety of

Ethernet standards that govern serial transmissions within a communication system at data rates of 10 megabits-persecond, 100 megabits-per-second, 1 gigabit-per-second and beyond. Synchronous Optical NETwork (SONET), for example, currently provides for up to 10 gigabits-per-second. In accordance with such standards, many system components and end user devices of a communication system transport data via serial transmission paths. Internally, however, the system components and end user devices may process data in a parallel manner. As such, each system component and end user device must receive the serial data and convert the serial data into parallel data without loss of information. After processing the data, the parallel data must be converted back to serial data for transmission without loss.

[0004] Accurate recovery of information from high-speed serial transmissions typically requires transceiver components that operate at clock speeds equal to or higher than the received serial data rate. Higher clock speeds limit the usefulness of prior art clock recovery circuits that require precise alignment of signals to recover clock and/or data. Higher data rates require greater bandwidth for a the feedback loop of the clock recovery circuits to operate correctly. Some prior art designs are bandwidth limited.

[0005] As the demand for data throughput increases, so do the demands on a high-speed serial transceiver. The increased throughput demands are pushing some current integrated circuit manufacturing processes to their operating limits, where integrated circuit processing limits (e.g., device parasitics, trace sizes, propagation delays, device sizes) and integrated circuit (IC) fabrication limits (e.g., IC layout, frequency response of the packaging, frequency response of bonding wires) limit the speed at which the high-speed serial transceiver may operate without excessive jitter performance and/or noise performance.

A further alternative for high-speed serial IUUU6)

A TUTCHET alternative for night-speed serial
transcelvers is to use an IC for instance awitching transcelvers for areater aneeds

provides For instance, switching from a Provides for greater speeds. For instance, switching in arsenide congress to a silicon germanium or gallium arsenide transfer to a silicon germanium or gallium or ga CMUS process to a silicon germanium or gallium arsenide transceivers to integrated circuit transceivers incress process would allow eneads but at enhotantially increase process at areater eneads process would allow integrated circuit transcelvers to increased but at substantially increased but at substantially and process would allow speeds, a more cost affective and operate at greater operate at greater operate at greater operate. x-1359 US operate at greater speeds, but at substantially increase operate at greater speeds, but at substantially increase operate at greater cmos is more cost effective and costs.

The substantial is more cost of the substantial increase of the substantial increase operate at greater costs.

The substantial increase operate of the substantial increase operate at substantial increase operate operate at substantial increase operate oper provides for greater speeds. Currently, for most provides easier system integrations, including communication

provides easier system integrations, including communication

commercial-grade applications, integrated circuit fahrication

commercial-grade applications, integrated circuit fahrication

commercial-grade applications, integrated circuit fahrication Commercial grace applications, including communication integrated circuit fabrication integrated circuit fabrication systems, such alternate prohibitive for wideenread use systems, are too nost prohibitive for wideenread use processes are too nost prohibitive for wideenread use processes are too nost prohibitive for wideenread use processes are too nost processes. systems, such alternate integrated circuit tabrication him includes prohibitive for widespread use. munutages easier system integration.

provides easier are too cost pronintative for widespread high data including high data including high data.

Modern communication systems. including high data including high data include a plurality of include a plurality of typically include a plurality of typically arch other hu way of rate communication systems, typically arch other hu way of circuit hoards that communicate with each other circuit hoards that communicate circuit circuit boards bundled data lines, back planes, carions signal traces, accommon of him data rate communicate with each other planes, carions as a signal traces, accommon of him data rate communicate with each other planes, carions as a signal traces, accommon of him data rate communicate with each other planes, carions and care and ca signal traces, designers of high data confliction designers of have confliction designers accordingly, devices of high data transceiver Accordingly, designers of high data rate communication that high data rate communication for high data rate communication for high data rate communication for the narricular device.

Accordingly, designers of the narricular device formance of the narricular devices transceiver the narrormance of the narricular devices. transceiver devices of the particular device.

transceiver the performance of the particular communication of the performance o relate to there are many that range from 2 49237 minahire example, for data rates example, there are many different communication protocols

there are many different communication protocols

that range from 2.48832 gigabits

example, there are many different communication protocols

there are many different communication protocols

example, the communication protocols

examp specified for data rates 9.95 gigabits per second for oclass that range from 2.48832 gigabits per second for oclass to 9.95 gigabits per of 2.5 gigabits per per second for oclass to 9.95 gigabits rates of 2.5 gigabits per conditions of the per second for OC48, to 9.95 gigabits per aerona (XANIT)

Per second for OC48, to define data rates of aerona (XANIT)

Other Known standards or 3 125 minahita ner aerona (TNETNTRANIT) Uther Known standards of 3.125 gigabits per second rice and second (INFINIBAND) or 3.125 gigabits per allowable rice and second (INFINIBAND) or affect the allowable rates affect the a These different data rates affect the allowante fise and the peak amplitude of the signal, the peak amplitude for example. Or the signal, the peak amplitude for example, or fall the resnonse time from an idle state. kor examble, oue and the response time from an idle state. For example and the response time a peak voltage range of 200-400 mirrial protocol may specify a peak randard enantial another erandard enantial another erandard enantial another erandard enantial another erandard enantial protocol may specity a peak voltage range of 200-400

protocol may specity a peak voltage specifies a mutually millivolte manue of son-700 millivolte male range of son-700 millivolte male manue of son-700 millivolte manue of son-700 mill and the response time from an idle state. exclusive voltage range of but these mutually exclusive designer land therefore cannot current multiple millivolts, while another standard specifies a manufacture of 500-700 millivolts.

exclusive voltage range of social accordance of soci designer elener cannot sacion a him data rate transceit requirements (and therefore a him data rate transceit requirements) requirements (and theretore cannot support multiple transceiver hains and theretore a high data rate protocols) or must design a high to the protocols or must according to the protocols or an adapt according to the protocols of protocols) or must design a high to the protocol being used to the protocol being to the protocol being device that can adapt according to the protocols or must design a high to the protocol being t Junual Callons. field programmable gate array

Along these lines, and a second a sec 100081 Circuits are gaining in popularity for providing the for the communications. 180001

required flexibility and adaptable performance described above for those designers that seek to build one device that can operate according to multiple protocols. Thus, while FPGA technology affords a designer an opportunity to develop flexible and configurable hardware circuits, specific designs that achieve the desired operations must still be developed.

One design challenge for serial data processing, [0009] especially for high data rate communications, relates to synchronization, and in particular to timing differences between a reference clock and high data rate serial stream. Such differences can lead to buffer overflows/underflows, unnecessary delays and other complications. The problem of synchronization mismatch become more acute in devices that conduct multi-gigabit serial data rates. For such systems, it is important to eliminate these mismatches because of the high volume of data being transported. In these systems especially, but more generally in all serial communication systems, even a mismatch of one percent can lead to buffer overflows/underflows and other problems. This problem of high data rate mismatch is a significant problem for any type of device or system that receives, processes or transmits high data rate serial data. A need exists, therefore, for a device and accompanying method with broad applicability that resolves high data rate mismatch between the data and a given clock used to operate upon or process the high serial rate data.

# BRIEF SUMMARY OF THE INVENTION

[0010] The present invention provides for a device and a method for processing high data rate serial data that reduces or eliminates mismatch between a reference clock and a high data rate serial data and the associated problems, including buffer overflow or underflow, that result therefrom. Generally, the invention includes circuitry for recovering a clock based on the high data rate input data

stream and for providing the recovered clock to a circuit portion, for example, a portion of a field programmable gate array fabric, to enable the circuit portion to use either a reference clock or the recovered clock for subsequent processing. The invention specifically allows for different circuitry portions to utilize different clocks for a corresponding function that is being performed.

Applications for the present invention are many but specifically include multi-gigabit transceiver, switching devices, protocol translation devices.

One embodiment of the present invention includes [0011] recovering a plurality of clocks from a corresponding plurality of serial data bit streams and using the plurality of recovered clocks to process each of the plurality of serial data bit streams in a corresponding functionality block. Another embodiment receives a high data rate serial data stream in a first protocol and translates the high serial data rate according to a recovered clock for the received high data rate serial data stream to a second protocol. Then, in one embodiment, the high data rate serial data stream in the second protocol is provided for transmission at the recovered clock rate. In an alternate embodiment, if the high data rate serial data stream is generated in the second protocol at a rate that is slightly different than the received data rate, the invention includes determining a corresponding clock and providing the high data rate serial data stream in the second protocol for transmission at a second recovered clock rate. It may be seen, therefore, that the invention includes circuitry and method for recovering and using a clock for a particular application to reduce timing mismatches. Further, the invention includes a device and method for recovering a plurality of clocks and performing a plurality of functions based on the plurality of recovered clocks concurrently.

rootal

Programmable logic device that includes multi-rinanit

Programmable logic device transfer multi-rinanit

Programmable logic of nronrammahla multi-rinanit BRIEF DESCRIPTION OF THE DRAWINGS programmable rogic device that includes programmable multi-gigabit
fabric, a plurality of programmable multi-gigabit Figure 2 is a schematic block diagram of one 100131

embodiment of a representative one of the programmable embodiment of a representative one of the programmable embodiment of a representative one of the programmable embodiment of transcraivers. x-1359 US transceivers (PMGT) and a control module; and transcervers; an alternate schematic block Figure 3 illustrates an alternate schematic block multi
rigare 3 illustrates an alternate schematic block multi
tion 3 illustrates an alternate schematic block multi
tion 3 illustrates an alternate schematic block multi
tion 3 illustrates an alternate schematic block

the programmable multi
diagram of a representative one of the programmable representative one of the programmable multiranscelvers;
Figure 4A illustrates a schematic block diagram of multi-gigabit transceivers; LUUISI

the programmable receive and and alore receive and alore r the programmable front-end, a data and clock recovery module, programmable front-end, and a data and clock recovery and a data and clock recovery module, and a garial-to-parallel module. lal-to-parallel module; a schematic block diagram of recording the individual and recording the individ 100161

Rigure 4B LLiustrates a schematic plock a phase that includes a rarallal-to-carial module and line and line arallal-to-carial module aprogrammable rarallal-to-carial module aprogrammable carallal-to-carial module aprogrammable carallal-to-carial module aprogrammable carallal-to-carial module aprogrammable carallal-to-carial module carallal-to-carial carallal-to-carial-to-carial carallal-to-carial carallal-to-ca gigabit transceivers; a programmable transmit PMA module that includes a phase driver; and line driver; and line driver; and looked looked similar a parallel formational and looked similar and looked simila op, a parallel-to-serial module, and line orlver; a functional plock of a figure serial module, and of a parallel-to-serial module, and plock of a functional plock of a functio and a serial-to-parallel module; 100171

Figure 5 is a one of a plurality of clocks

transceiver to one amhodiment of the invention: to one embodiment of the inventioni diagram hand block of clock frigure inclinational triversity. cranscelver that selects one the invention; according to one embodiment of the invention; transceiver that each selects of the invention:

transceiver that each selects of the invention: 100181 Figure 6 is a tunctional plock of clock of plurality of a niurality of a niurality that transceiver that each ealents one of a finctional transceiver trans tunctionalities that each selects of the invention;

tunctionalities to one embodiment of himself one of a plural

to one of a plural

that each selects of the invention;

that each selects of the invention;

that each selects of the invention;

to one embodiment of himself one;

tunctionalities to one embodiment of himself one;

tunctionalities according to one embodiment of himself one;

tuncti coraing to one embodiment of the invention;

Figure 7 is a functional functio transceiver that that each ouraning serial data on a ninrality of that that ouraning serial data on a clocks for providing ouraning serial data on a clocks rigure 7 is a functional plock of clock

fincludes a plurality of animality

that pach calcute one of a that that pach calcute

transcelver transcelve functionalities that each selects one of a plurality of an one of a plurality of an one of a plurality of an aspect of an one of a plurality of of a plural clocks for providing outgoing serial data on a spect of an clocks for providing nodules according accordin t or the present inventional block diagram clocks functional nursality of Figure 8 is a one of a nursality of reacts and of a nursality of reacts one of a nursality of reacts. transceiver that selects of the invention wherein one of a plurality of clocks one of a plurality of one of the invention wherein one according to one embodiment of the invention wherein one according to one of the invention wherein one of the inve could that amondinant of the invention wherein transceiver to one amondinant of the invention wherein embodiment of the present invention;

the plurality of clocks is a recovered clock for a TX serial data stream;

[0021] Figure 9 is illustrates a block diagram of a clock and/or data recovery circuit in accordance with one embodiment of the present invention;

[0022] Figure 10 illustrates a schematic block diagram of a clock data recovery block of a transceiver with a coarse and a fine phase-locked loop according to one embodiment of the present invention;

[0023] Figure 11 illustrates a method for processing high data rate serial data according to a first embodiment of the invention;

[0024] Figure 12 illustrates a method of processing high data rate serial data according to a second embodiment of the invention;

[0025] Figure 13 illustrates a method of clock management according to a third embodiment of the invention; and [0026] Figure 14 illustrates a method of clock management according to a fourth embodiment of the invention.

# DETAILED DESCRIPTION OF THE INVENTION

[0027] Figure 1 is a schematic block diagram of a programmable logic device 10 that includes programmable logic fabric 12, a plurality of programmable multi-gigabit transceivers (PMGT) 14-28 and a control module 30. The programmable logic device 10 may be a programmable logic array device, a programmable array logic device, an erasable programmable logic device, and/or a field programmable gate array (FPGA). When the programmable logic device 10 is an FPGA, the programmable logic fabric 12 may be implemented as a symmetric array configuration, a row-based configuration, a sea-of-gates configuration, and/or a hierarchical programmable logic device configuration. The programmable logic fabric 12 may further include at least one dedicated fixed processor, such as a microprocessor core, to further

facilitate the programmable flexibility offered by a programmable logic device 10.

[0028] The control module 30 may be contained within the programmable logic fabric 12 or it may be a separate module. In either implementation, the control module 30 generates the control signals to program each of the transmit and receive sections of the programmable multi-gigabit transceivers 14-28. In general, each of the programmable multi-gigabit transceivers 14-28 performs a serial-to-parallel conversion on receive data and performs a parallel-to-serial conversion on transmit data. The parallel data may be, for instance, 8-bits, 16-bits, 32-bits, or 64-bits, wide.

[0029] Typically, the serial data will be a 1-bit stream of data that may be a binary level signal, multi-level signal, etc. Further, two or more programmable multi-gigabit transceivers may be bonded together to provide greater transmitting speeds. For example, if programmable multi-gigabit transceivers 14, 16 and 18 are transceiving data at 3.125 gigabits-per-second, the transceivers 14-18 may be bonded together such that the effective serial rate is approximately 3 times 3.125 gigabits-per-second.

[0030] Each of the programmable multi-gigabit transceivers 14-28 may be individually programmed to conform to separate standards. In addition, the transmit path and receive path of each multi-gigabit transceiver 14-28 may be separately programmed such that the transmit path of a transceiver is supporting one standard while the receive path of the same transceiver is supporting a different standard. Further, the serial rates of the transmit path and receive path may be programmed, for example, from 1 gigabit-per-second to tens of gigabits-per-second. The size of the parallel data in the transmit and receive sections, or paths, is also programmable and may vary, for instance, from 8-bits, 16-bits, 32-bits, or 64-bits.

Figure 2 is a schematic block diagram of one embodiment of a representative one of the programmable multi-gigabit transceivers 14-28. As shown, the programmable multi-gigabit transceiver includes a programmable physical media attachment (PMA) module 32, a programmable physical coding sub-layer (PCS) module 34, a programmable interface 36, a control module 35, a PMA memory mapping register 45 and a PCS register 55. The control module 35, based on the desired mode of operation for the individual programmable multi-gigabit transceiver 14-28, generates a programmed deserialization setting 66, a programmed serialization setting 64, a receive PMA\_PCS interface setting 62, a transmit PMA\_PCS interface setting 60, and a logic interface setting 58. The control module 35 may be a separate device within each of the multi-gigabit transceivers or included partially or entirely within the control module 30.

[0032] In either embodiment of the control module 35, the programmable logic device control module 30 determines the corresponding overall desired operating conditions for the programmable logic device 10 and provides the corresponding operating parameters for a given programmable multi-gigabit transceiver to its control module 35, which generates the settings 58-66.

module 32 includes a programmable transmit PMA module 38 and a programmable receive PMA module 40. The programmable transmit PMA module 38, which will be described in greater detail with reference to Figure 4B, is operably coupled to convert transmit parallel data 48 into transmit serial data 50 in accordance with the programmed serialization setting 64. The programmed serialization setting 64 indicates the desired rate of the transmit serial data 50, the desired rate of the transmit parallel data 48, and the data width of the transmit parallel data 48. The programmable receive PMA module 40, is operably coupled to convert receive serial

data 52 into receive parallel data 54 based on the programmed deserialization setting 66. The programmed deserialization setting 66 indicates the rate of the receive serial data 52, the desired rate of the receive parallel data 54, and the data width of the receive parallel data 54. The PMA memory mapping register 45 may store the serialization setting 64 and the deserialization setting 66.

The programmable physical coding sub-layer (PCS) module 34 includes a programmable transmit PCS module 42 and a programmable receive PCS module 44. The programmable transmit PCS module 42, receives transmit data words 46 from the programmable logic fabric 12 via the programmable interface 36 and converts them into the transmit parallel data 48 in accordance with the transmit PMA\_PCS interface setting 60. The transmit PMA\_PCS interface setting 60 indicates the rate of the transmit data words 46, the size of the transmit data words (e.g., 1-byte, 2-bytes, 3-bytes, 4-bytes) and the corresponding transmission rate of the transmit parallel data 48. The programmable receive PCS module 44, converts the receive parallel data 54 into receive data words 56 in accordance with the receive PMA\_PCS interface setting 62. The receive PMA\_PCS interface setting 62 indicates the rate at which the receive parallel data 54 will be received, the width of the receive parallel data 54, the transmit rate of the receive data words 56 and the word size of the receive data words 56.

[0035] The control module 35 also generates the logic interface setting 58 that provides the rates at which the transmit data words 46 and receive data words 56 will be transceived with the programmable logic fabric 12. Note that the transmit data words 46 may be received from the programmable logic fabric 12 at a different rate than the receive data words 56 are provided to the programmable logic fabric 12.

[0036] As one of average skill in the art will appreciate, each of the modules within the PMA module 32 and

PCS module 34 may be individually programmed to support a may he are transfer rate who have transfer rate who have transfer rate are transfer rate. The data transfer rate may be desired data transfer rate. The data transfer that receive nath a coordance with a particular standard normania transfer rate. The nath through normania transfer rate may the data tra in accordance with a particular standard such that receive pcs module 44 median accordance i.e., the path through receive pcs module i.e., the programmable receive pcs module i.e., and the path pma module 40 and the pma receive path, i.e., the path through programmable receive pcs module the programmable receive path, i.e., the programmable receive pcs module the programmable receive path, i.e., the programmable receive pcs module the programmable receive path, i.e., the programmable receive pcs module the pc PMA module 40 and the programmable receive kis module the be programmed in accordance with one arrangement the programmed in accordance through the arrangement of the programmed in accordance through the accordance to the accordance through the accordance to the ac be programmed in accordance with one standard while transmit the programmable transmit pwn module 38 transmit pwn module 42 and the programmable transmit programmable transmit pwn module transmit pwn module transmit pwn module 42 and the programmable transmit pwn module transmit pw desired data transfer rate. x-1359 US transmit path, i.e., path through the programmable transmit pMA module 38

transmit path, i.e., programmable transmit pMA module 38

pcs module 42 and the programmable with the earn or another may be programmad in accordance with the earn of another may be programmad in accordance with the earn of another may be programmad. may be programmed in accordance with the same or another Rigure 3 illustrates an alternate schematic block Luus II of a representative one of the programmant the diagram of a representative one of the programmant of a representative one of the programmant the or this ambout mant of a representative one of the programmant the order of diagram of a representative one of the programmable my the In this embodiment, includes for 14-28. Transceiver 14-28 transceiver 14-28 transceiver and includes gigabit transceiver milti-minahit milt glgapit transcelvers 14-28.

In this embodiment, the includes a la-28 includes a receiver 14-28 includes a receiver 17 transcelver 72 transcelver 73 transcelver 72 transcelver 73 transcelver 73 transcelver 73 transcelver 74 transcelver 75 transce transmit section 70, a receive section 36. The module 35 and the programmable interface transmit pma module 35 and the programmable transmit pma module 35 and the programmable transmit pma nromrammable transmit pma module 35 and the programmable transmit pma nromrammable transmit pma module 35 and the programmable transmit pma nromrammable transmit pma module 35 and the programmable transmit pma nromrammable transmit pma module 35 and the programmable transmit pma module 36. module 35 and the programmable interface 36. The transmit man receive module 35 and the programmable transmit man receive section 70 includes transmit pre module 47 manual programmable transmit pre module 47 and the programmable transmit pre module 47 and the programmable transmit pre module 47 and the programmable transmit pre module 48 and the programmable transmit pre module 48 and the programmable transmit pre module 35 and the programmable transmit pre module 38 and the programmable interface 36. The programmable interface 40 and 10 and standard. and the programmable transmit programmable receive the programmable at module 42.

section 72 includes receive programmable receive programmable and the programmable receive and the programmable receive 40. 100311 section in incinces the programmable transmit PCS module 42. in this embodiment, the control module 35 receive the transmit section and the receive retrieve and receive retrieve and receive retrieve retrieve the transmit separately programs the transmit earthing in the transmit earthing in the transmit earthing in the control module 35 receive receiver receive receive receiver receive receive receiver receiver receive receiver recei In this embodiment, the control module 35 and the programmable receive pcs module 44. separately programs the transmit section and the receive that the transmit section and the receive that the transmit section and receive setting the transmit setting 74 and receive normana the transmit section and receive transmit section making as also normana the receive that the receive section and the receive that the receive section and the receive that the receive section and the receive that the receive that the receive section and the receive that the receiv section via transmit setting 14 and receive setting the module 35 also programs eart;

The control module 100 interface 36 via the 100 interface art;

respectively. respectively.

The control module 30 also programs setting interface setting the logic interface represents the programmable interface represents the control module 35 may programmable interface represents the control module 35 may programmable and represents the control module 35 may programmable and represents the control module 35 may programmable and represents the control module 35 may programs the control module 35 also programs the control module 35 a rammable interface 30 via the Logic interface setting the control module 35 may program the the control module 35 may program the Accordingly.

Accordingly to function in accordance with one 58. Accordingly, the control module 35 may program the function in accordance with one in accordance with one function in accordance with one function in accordance with one in accordance with a contract with a contract with accordance with accordance with a contract wit receive section programming the transmit section programming or another etandard while programming the standard with the earne or another standard with the earne or another etandard standard with the earne or another etandard etandard with the earne or another etandard accordance with the same or another standard. the transmit indicate that the logic interface setting the from the arrangement of the logic interface are received from the arrangement of the logic works. Further! stanuaru with the same co mair indicate that accordance with action co mair indicate accordance with the same co mair indicate that accordance with the same co mair indicate that accordance with the same co mair indicate that the accordance with the same co mair indicate that the same committees that the same contains the same c logic intertace setting by may indicate that the logic that the programmable hat we have the programmable had been programmable as the programmable had been pro data words 46 are received from the programmable logic As or late words a different rate than logic fabric 12 at a different range and the received from the received data words fabric 12 at a different range and the received from the programmable logic as or some fabric 12 at a different range and the received from the programmable logic data words fabric 12 at a different range are received from the programmable logic data words are received from the received data words are received from the received data words are received from the received from the received data words are received from the As one tabric 12 at a different rate than the received data we take the programmable logic fabric 12.

tabric 12 at a different rate programmable logic fabric the programmable annraniate that the programmable annraniate that the programmable logic fabric fa of average skill in the art will appreciate, the buffer and include a transmit hoffer to average skill in the 36 may include arore hiffer to programmable interface and/or an elactic arore hiffer and/or are are are around the arore hiffer and/or an elactic arore hiffer and/or are are around the ar bo are provided to the programmable logic rabric in the art will appreciate, the of average skill in the art will appreciate, are now, include a transmit programmable incertace so may include a cransmic buller to an elastic store buffer to a receive buffer.

facilitate the providing and receiving of the data words 46 and 56 to -and from the programmable logic fabric 12.

[0039] Figure 4A illustrates a schematic block diagram of the programmable receive PMA module 40 that includes a programmable front-end 100, a data and clock recovery module 102, and a serial-to-parallel module 104. The programmable front-end 100 includes a receiver termination circuit 106 and a receiver amplifier 108. The data and clock recovery module 102 includes a data detection circuit 110 and a phase locked loop 112. The phase locked loop 112 includes a phase detection module 114, a loop filter 116, a voltage controlled oscillator 118, a 1st divider module 120, and a 2nd divider module 122.

The programmable front-end 100 is operably coupled [0040] to receive the receive serial data 52 and produce amplified and equalized receive serial data 124 therefrom. To achieve this, the receiver termination circuit 106 is programmed in accordance with a receive termination setting 126 to provide the appropriate termination for the transmission line between the programmable receiver PMA module 40 and the source that originally transmitted the receive serial data The receive termination setting 126 may indicate whether the receive serial data 52 is a single-ended signal, a differential signal, may indicate the impedance of the transmission line, and may indicate the biasing of the receiver termination circuit 106. For a more detailed discussion of the receiver termination circuit 106 refer to co-pending patent application entitled "RECEIVER TERMINATION -NETWORK AND APPLICATION THEREOF" by Charles W. Boecker, William C. Black, and Eric D. Groen , having the same filing date as the present application, which is hereby incorporated by reference in its entirety.

[0041] The receiver termination circuit 106 further biases the receive serial data 52 and provides the bias adjusted signal to the receiver amplifier 108. The equalization and gain settings of the receiver amplifier 108

may be adjusted in accordance with equalization setting 128 and amplification setting 130, respectively. Further description of the receiver amplifier 108 may be found in co-pending patent application entitled "ANALOG FRONT-END HAVING BUILT-IN EQUALIZATION AND APPLICATIONS THEREOF" by William C. Black, Charles W. Boecker, and Eric D. Groen , having a filing date the same as the present patent application, which is hereby incorporated by reference in its entirety. Note that the receiver termination setting 126, the equalization setting 128, and the amplification setting 130 are part of the programmed descrialization setting 66 provided by the control module 35.

The data and clock recovery circuit 102 receives [0042] the amplified and equalized receive serial data 124 via the phase detection module 114 of phase locked loop 112 and via the data detection circuit 110. The phase detection module 114 has been initialized prior to receiving the amplified and equalized receive serial data 124 by comparing the phase and/or frequency of a reference clock 86 with a feedback reference clock produced by divider module 120. this phase and/or frequency difference, the phase detection module 114 produces a corresponding current that is provided to loop filter 116. The loop filter 116 converts the current into a control voltage that adjusts the output frequency of the voltage controlled oscillator 118. divider module 120, based on a serial receive clock setting 132, divides the output oscillation produced by the VCO 118 to produce the feedback signal. Once the amplified and equalized receive serial data 124 is received, the phase detection module 114 compares the phase of the amplified and equalized receive serial data 124 with the phase of the feedback signal, and produces a current signal based on the phase difference.

[0043] The phase detection module 114 provides the current signal to the loop filter 116, which converts it into a control voltage that controls the output frequency of

the voltage controlled oscillator 118. At this point, the controlled oscillator 118. At this point, the national oscillator 118. the voltage controlled oscillator 118. At this point, the man at this point, the corresponds are at this point, and this point, the corresponds are at this point, and the corresponds are at the co recovered clock 138is provided to the divider module 1221, the the serial-to-parallel to the serial-to-parallel to the serial-to-parallel the data detection circuit 110 and to the serial to the seri the data detection circuit 110 and to the serial-to-parall and to the serial-to-parall and to the serial-to-parall the data detection circuit 110 whilizes from the module 104. module 104.

The data detection circuit 110 utilizes the man are arrive aerial data 124

The data detection recovered data 124

The data data data data 124

The data data data data 124

The data data data 124

The data data data data 124

The data data data 124

The data data data 124

The data data data data 124

The data data 124

The data data data 124

The data data data 124

The data da x-1359 US recovered clock libb to recover recovered data 124.

amplified and equalized receive serial data and amplified and an analysis amplified and equalized receive serial data 124. In an arange in a receive and aroung amplified and equalized divides the recovered and aroung amplified and 122 divides receive and aroung amplified and equalized areas are also as a serial data and equalized receive serial data 124. divider module 124 to produce the parallel receive and programmable alvides the receive and programmable alvides the parallel receive and parallel receive alvides the parallel receive and programmable alvides the parallel receive alvides t accordance with a parallel receive and programmable logic 94 note that the note that the logic parallel receive and programmable receive that the parallel receive clock 96. clock setting 134, to produce the parallel receive that the normal logic receive clock 96.

clock setting logic receive clock and the narrallel receive and a programmable clock setting logic receive clock 96. and a programmable clock setting 132 and the parallel receive clock setting 134 are nart of the setting 134 are na serial receive clock setting 132 and the parallel receive and programmed Asearialination earting around the parallel receive the setting 134 are part of the setting for a consideration and programmed Asearialination earting for a consideration earting for a programmed deserialization setting 66 provided to the 35.

programmed deserialization module 40 by the control module 104 which may programmable receive pwA module module 104 which may programmable arrial-to-narallal module 35. and programmable logic clock setting 66 provided to modification s The serial-to-parallel module 104, which may data recovered clock the recovered clock buffer, receives the recovered clock in accordance with the recovered clock include an elastic store in accordance with the recovered clock are a serial rate in accordance with the recovered clock with the recovered clock are a serial rate in accordance with the recovered clock include an elastic store in accordance with the recovered clock include an elastic store in accordance with the recovered clock include an elastic store in accordance with the recovered clock include an elastic store in accordance with the recovered clock include an elastic store in accordance with the recovered clock include an elastic store in accordance with the recovered clock include an elastic store in accordance with the recovered clock include an elastic store in accordance with the recovered clock include an elastic store in accordance with the recovered clock include an elastic store in accordance with the recovered clock include an elastic store in accordance with the recovered clock include an elastic store in accordance with the recovered clock include an elastic store in accordance with the recovered clock include an elastic store in accordance with the recovered clock include an elastic store in accordance with the recovered clock include an elastic store in accordance with the recovered clock include an elastic store in accordance with the recovered clock include an elastic store in accordance with the recovered clock in the recovered clock include an elastic store buffer, receives the recovered clock in accordance with the rate in accordance with the r Liv. Based on a serial-to-parallel serting liss and the module serial-to-parallel module managed on a serial-to-parallel serial-to-parallel managed on a serial-to-parallel serial-to-parallel managed on a serial-to-parallel serting liss and the managed on a serial-to-parallel serting liss and the managed on a serial-to-parallel serting list and managed on a serial-to-parallel sertial-to-parallel serial-to-parallel sertial-to-parallel serial-to-parallel s Tua outputs the receive parallel data sa the programmed which may be part the data rate and de part the data rate and de parallel setting parallel setting serring ser parallel setting 135, which may be part of the programmed at a rate and data for the programmed at a parallel data for the programmed at a paralle pararier receive receive parallel data 54. Life receive parallel vala 34.

Rigure 48 illustrates a schematic block diagram of the figure 48 illustrates a schematic rigure 4B illustrates a schematic block diagram of includes a phase transmit pwa module 38 that includes and line and line argument transmit pwa module argument a programmable a parallal to serial module a parallal to seri a programmable transmit PMA module 38 that includes a phase nhaep nodule 38 that includes a phase and line aparallel-to-serial module includes a nhaep nhaep locked loop nhaep looked loop nhaep loop nhaep looked loop nhaep looked loop nhaep loop nhaep looked loop nhaep width of the receive parallel data 54. driver 142. The phase locked loop 141 a loop filter 154.

driver 142. The phase a charge pump 147 a divider module 166 a charge pump 150. a divider module detection module oscillator 150. a divider module detection a divider module detection module oscillator 150. detection module 146, a charge pump 14, a divider module 154, a divider module 150, a divider module 160 a voltage controlled oscillator 150, a divider module 160 a voltage a voltage a divider module 160 a voltage controlled 160 a voltage control The phase detection module 146 compares the phase luusol

The phase detection module 140 compares the phase with the phase of the reference clock 86 with the phase of the reference crowned my divider module and or framework of an ourmit oroduced my divider module and or framework of an ourmit oroduced my divider module and or framework of an ourmit oroduced my divider module and or framework of an ourmit oroduced my divider module 140 compares the phase with the phase of the reference clock 86 with the phase of the reference clock 96 with the phase of the reference 16 with the phase of the reference clock 96 with the phase of the reference clock 96 with and/or trequency of an output produced by divider module and/or frequency of an arrange and/or make abtain module r requency or an output produced by alvider module requency or an output produced by all alvider module requency or an output produced by alvider module requency or an output produced by all alvider module requency or an output produced by all alvider module requency or an output produced by all alvider module requency of the driver 142. and a divider module 152. 100461

signals to charge pump 147 which, in turn, produces a current signal to represent the phase and/or frequency difference between the reference clock 86 and the feedback oscillation. The loop filter 148 converts the current signal into a control voltage that regulates the output oscillation produced by the voltage controlled oscillator 150. Divider module 154, based on a serial transmit clock setting 158, divides the output oscillation of the VCO 150, which corresponds to the serial transmit clock 92, to produce the feedback oscillation. Note that the serial transmit clock setting 158 may be part of the programmed serialization setting 64 provided to the programmable transmit PMA module 38 by the control module 35.

[0047] Divider module 152 receives the serial transmit clock 92 and, based on a parallel transmit and programmable logic clock setting 160, produces the parallel transmit clock 88 and the transmit programmable logic clock 90. The parallel transmit and programmable logic clock setting 160 may be part of the programmed serialization setting 64.

[0048] The parallel-to-serial module 140 receives the transmit parallel data 48 and produces therefrom a serial data stream 156. To facilitate the parallel-to-serial conversion, the parallel-to-serial module 140, which may include an elastic store buffer, receives a parallel-to-serial setting to indicate the width of the transmit parallel data 48 and the rate of the transmit parallel data, which corresponds to the parallel transmit clock 88. Based on the parallel-to-serial setting, the serial transmit clock 92 and the parallel transmit clock 88, the parallel-to-serial module 140 produces the serial data stream 156 from the transmit parallel data 48.

[0049] The line driver 142 increases the power of the signals forming serial data stream 156 to produce the transmit serial data 50. The line driver 142, which is described in greater detail in co-pending patent applications related applications listed above and having

the same filing date as the present application, may be the same filing date as the present application, alow rate or adjust its pre-amphasis sattings. the same filing date as the present application, may be rate its pre-emphasis settings, control arrive carring via a nre-emphasis control programmed to adjust carring via a nre-emphasis control carring via a nre-emphasis carring via a n programmed to addust its pre-emphasis settings via a pre-emphasis a alew resettings and drive settings earting eignal 169 settings. settings, and drive settings via a pre-emphasis aslew rate signal 162, and a drive setting signal 165, and a drive signal 161, a pre-emphasis setting serving 161, a pre-emphasis setting serving 161, and 164, and 164 and 16 signal lol, a pre-emphasis setting signal lol, a pre-emphasis setting setting los and a drive state setting los and a drive signal lol, a pre-emphasis state setting control signal lol, and a drive setting signal lol, a pre-emphasis setting signal lol, a pre-emphasis setting signal lol, a pre-emphasis setting setting signal lol, a pre-emphasis setting setting signal lol, and a drive setting setting signal lol, and a drive setting signal lol, a pre-emphasis setting setting signal lol, and lol, a setting signal 164, an idle state setting 165 and a drive state setting 165 and a drive state setting 165 and a drive setting 165 and a drive setting 166. The pre-emphasis control signal 166. The pre-emphasis current setting 166. Signal 167 the slew rate setting current setting setting 167. current setting 166. The pre-emphasis slew rate setting or are corring 166. The signal rate setting or are corring 166 and the arm of the setting or are corring 166 and the drive of the setting or are corring 166 and the drive of the setting or are corring 166 and the drive of the setting or are corring 166 and the drive of the setting or are corring 166 and the drive of the setting of the set Pre-emphasis setting signal 162, the slew rate setting 163 and the drive current 162, the slew rate setting 165 and the drive current 164, the idle state setting 164, the idle part of the programmed serialization signal 164, may be part of the certain 16 x-1359 US signal 104, the 101e state setting 165 and the drive curr

the programmed serialization

setting 166 may be part of average evill in the art will

setting 64 as one of average evill setting 100 may be part of the programmed serialization of the setting by. As one of average skill in the art will as a different will as a different will as a different average skill in the art will average skill in the art will be different average skill in the art will be different average skill in t appreciate, while the diagram of rigure and use differential and singlethe entire of differential and singlesingle-ended system, combination of differential and singlesingle-ended and/or a combination single-ended system, the entire system may use differential and singlesignaling and/or a combination of differential and signaling and/or a combination of differential and singlesignaling and/or a combination of differential and singleended system, the entire system may use differential and singleended system, the entire system may use differential and singleended system, the entire system may use differential. Figure 5 is a functional block diagram of a 100501 transceiver 170 one amandiment of transceiver to one amandiment of transceiver transceiver transceiver to one of the transceiver transceiver transceiver to one of the transceiver transc transceiver 170 that selects one of the invention.

transceiver one embodiment of the invention or a processor hasped according to one embodiment an acro according to one an acro according to one an acro an acro an acro an acro according to one according to one an acro an acro according to one embodiment of the invention.

A transceiver

A tr IN may be tormed as an Asici an thereof for performing a device, or any combination to the avample of rimine device, any combination device, or any combination thereof for pertorming a the examples of Figures FPCA (and Examples of Action and Experimental Specified function. specified function.

In the examples of Figures 5-8, the fixed and FPGA (e.g., transceived function).

In the examples of ASIC and FPGA (e.g., transceived for a combination).

The examples of Figures 5-8, the fixed function.

The examples of ASIC and FPGA (e.g., function).

The examples of Figures 5-8, the fixed function.

The examples of Figures 5-8, the fixed function function.

The examples of Figures function function function.

The examples of Figures function functi ended signaling. In Figure 5, transceiver fixed and programmable) circuitry. In Figure 5, transcei.

In Figure 5, transcei. 170, which is for processing high data rate serial data, and the serial data rate serial data rate serial data, and the serial data rate serial data rate serial data rate serial data, and the serial data rate serial data, and the serial data rate serial data, and the serial data rate serial data. includes a first serial data 52A from a receiver and for nroviding receiving a receiver a receiver and for nroviding receiving and for nroviding receiving and for nroviding receiving programmable received by the nroviding receiving programmable received by the nroviding receiving programmable received by the nroviding received by the nroviding received by the nroviding received block such that the nroviding received block such a receiver block such are received block such as a first clock data from a receiver and and for nroviding receiver and the nrovidi receiving first serial data 52A from a receiver providing a module 40A and for providing a neceiving first serial data 52A module serial data 52A from the first serial data 62A from the claus end programmable) circultry. as a programmable receive run module serial data data data to provide as a programmable receive run the first seamed clock from the first recovered clock from the first recovered further includes a seamed clock from the first recovered further includes a seamed clock from the first recovered further includes a seamed clock from the first recovered to the first reco transceiver 170 further includes a second clock data data 52B includes a second serial data pmA

transceiver 170 further for receiving second receive pmA

transceiver circuitry 174 for receiven as a nromrammable receiver recovery receiver ninck such as a nromrammable ninck such as a n first recovered clock from the tirst serial data data as second clock data as second clock from the tirst second clock data as second clock from the tirst second clock data as second clock from the tirst second clock data as second clock data as second clock data as second clock from the tirst second clock data as second c recovery circuitry block such as a programmable receive from a receiver for nrowiding a conna recovery from a Ang and for nrowiding a conna recovery such as a programmable receiver block such as a programmable receiver block such as a conna recovery circuitry block such as a conna recovery circuitry block such as a conna recovery circuitry block such as a programmable receiver block such as a programmable receiver block such as a conna recovery circuitry block such as a programmable receiver block such as a programmable receive from a receiver block such as a programmable receiver block such as a conna receiver bloc from a receiver block such as a programmable receive pwa.

from a receiver block such as a second recovered clock from a second further gransceiver 170 further gransceiver 170 further are module 40B and for providing gransceiver 170 further gransceiver gransceiver 170 further gransceiver 170 further gransceiver gransceiver 170 further gransceiver grans module 40B and for providing a second recovered clock gransceiver 170 further a meansceiver normalism and for providing a second recovered clock gransceiver 170 further a module 40B and for providing a second recovered clock gransceiver normalism a second reference clock module 176 for normalism and the second reference clock module 176 for normalism and the second reference clock gransceiver and the second recovered clock as second recovered clock gransceiver and the second grant gransceiver and grant gransceiver and grant includes a reference clock module 176 for providing a first reference clock module 176 for providing a first reference clock and the reference clock and reference all provided to provide and recovered clocks are all provided to provide and second recovered clocks. the second serial data 528. Transcelver providing a north and the includes a reference clock man reference clock includes a range clock and the reference clock and the refere reference clock signal.

The reference clock and the first programmable programmable provided to programmable provided to programmable programmable programmable are all provided to programmable programmable programmable programmable programmable interface and second recovered programmable locations are all programmable programma and second recovered clocks are all provided to programmable programmable logic fabric 12.

logic fabric 12 receives each recovered clock and reference clock produced to it and routes the clock to specified functionalities within the logic fabric as specified by the programmable logic. Additionally, each serial data stream, here RX serial data streams 52A and 52B, are also provided to programmable interface 36 of programmable logic fabric 12.

The programmable logic fabric 12 includes a [0051] plurality of clock based functionalities illustrated herein as clock based functionalities 178, 180 and 182. Each of the first and second recovered clocks and the reference clock is provided to a circuit portion of the transceiver wherein the circuit portion chooses among the first and second recovered clocks and the reference clock for subsequent processing by at least one clock based functionality (here, by the three clock based functionalities 178, 180 and 182). For example, in the embodiment of invention shown in Figure 5, the first and second recovered clocks and the reference clock are provided to the programmable interface 36 of the programmable logic fabric 12. Each clock based functionality selects one of the clocks provided to the programmable interface 36 (e.g., one of the first and second recovered clocks and the reference clock) and, based on the selected clock, performs subsequent specified functions.

[0052] In the described embodiment of Figure 5, transceiver 170 includes at least three clock based functionalities 178, 180 and 182, respectively. Each functionality 178, 180 and 182 selects a clock for its functionality and thus may operate according to different clocks in relation to each other. In the described embodiment, each functionality 178, 180 and 182 selects a specified recovered clock according to programming or internal logic. While each clock based functionality 178, 180 and 182 is shown within programmable logic fabric 12, they may readily be formed external to such fabric 12 and

may, for example, be formed out of and as a part of application specific integrated circuitry or other logic circuitry. Each functionality 178, 180 and 182 includes circuitry for performing a specified task, which may include tasks relating to high rate serial data processing.

[0053] More generally, the invention shown in Figure 5 illustrates the generation of a plurality of clocks and selectively performing specified functions based on any one or more of the plurality of clocks. Thus, the invention includes performing functions that are synchronized in time with the data for which the function is being performed. By separating functionality from a system clock or reference clock, and by synchronizing the functionality with a clock within a serial data transmission, a need for large buffers and the possibility of buffer overflows/underflows due to mismatches in the reference clock and the data stream rate is avoided or at least reduced.

[0054] Figure 6 is a functional block diagram of a transceiver 184 that includes a plurality of clock based functionalities that each selects one of a plurality of recovered or reference clocks according to one embodiment of the invention. Transceiver 184, in comparison to transceiver 170, includes third clock data recovery circuitry 186 for receiving RX serial data 52C from a third programmable receive PMA module 40C and for providing a third recovered clock to programmable interface 36 of programmable logic fabric 12. Additionally, a transmitter clock 187 produces a transmit reference clock signal to programmable interface 36. Generally, a transmit reference clock is merely a clock, perhaps a recovered clock, for a serial data stream that is to be provided by the transceiver, here, transceiver 184. For example, if a serial data stream is being provided for transmission at a specified rate, the transmit reference clock reflects a clock rate of the transmit data as it is being provided, and

may be provided to a functionality for processing at the specified transmit clock rate.

[0055] Programmable logic fabric 12 of transceiver 184 provides each received input serial data stream of the plurality of input serial data streams to a specified outgoing transmit block based upon a clock that is recovered from the corresponding input serial data streams. specifically, in the example shown, the transmit blocks include programmable transmit PMA modules 192A, 192B and 192C. Alternatively, each of these transmit blocks may readily be a transmitter port, for example. described example, any one of the clock based functionalities 178, 180 and 182 processes any one of the received RX serial data streams 52A, 52B and 52C based upon a corresponding recovered clock according to specified logic or programming. In the example herein, transmit functionality 190 provides the TX serial data 188A, 188B and 188C to the corresponding programmable transmit PMA module 192A, 192B and 192C according to the corresponding recovered clocks (with which the functionality processed the data). Generally, Figure 6 illustrates that a plurality

of functionalities, including one or more transmit functionalities, may process a serial data stream according either to a recovered clock of the data, a reference clock, or a transmitter clock as described before. Further, Figure 6 illustrates that the different functionalities may operate according to the different clocks in a concurrent manner.

Figure 6 further illustrates use of an embodiment of the present invention in a switching application. be seen, three serial data streams are received and are provided to a selected output port. Thus, the clock based functionalities may be as simple as routing the received serial data streams to selected output ports or transmit PMA In general, a clock is recovered from each of the input data streams and is used for routing and producing output data streams. By routing and transmitting each

according to a corresponding recovered clock rate, significant timing problems, including buffer overflow/underflow problems, are reduced or eliminated. should be understood that Figure 6 merely shows three input and three output serial data streams but that the invention is not so limited and includes any number of each. example, first CDR 172 provides a recovered clock for RX serial data 52A to programmable logic fabric 12. PMA 32 provides RX serial data 52A to first CDR 172 as well as to programmable logic fabric 12 by way of programmable interface 36. Thereafter, a specified functionality, such as functionality 178 provides selected clock based serial data 188A. The selected clock may be the first recovered clock provided by first CDR 172 or any other selected clock including the reference clock.

Figure 7 is a functional block diagram of a [0058] transceiver 194 that includes a plurality of clock based functionalities that each selects one of a plurality of clocks for producing outgoing serial data on a plurality of data ports or modules according to one aspect of an embodiment of the present invention. In contrast to transceiver 184 of Figure 6 and to transceiver 170 of Figure 5, transceiver 194 of Figure 7 further includes a transmit port 196 at which a serial data stream may be provided. operation, transmit functionality 190 provides selected clock based TX serial data 188 to transmit port 192 and selected clock based TX serial data 197 to programmable transmit PMA module 196 according to specified logic defined within transmit functionality 190.

[0059] Figure 8 is a functional block diagram of a transceiver 198 that selects one of a plurality of clocks according to one embodiment of the invention wherein one of the plurality of clocks is a recovered clock for an I/O serial data stream 51. Generally, I/O (input/output) serial data stream 51 represents any serial data stream including a received serial data stream, or an outgoing serial data

stream being generated at a specified rate. A transceiver 198 includes a selectable clock based functionality 200 within programmable logic fabric 12 that selects from (i) a first recovered clock provided by a first clock and data recovery circuit 172 that recovers a clock from serial I/O stream 51 or (ii) a second recovered clock provided by delay locked loop circuit 174 that recovers a clock from an RX serial data stream 52 and that compensates for downstream phase shifts. While in some applications, merely using a reference clock for outgoing transmissions is adequate, the embodiment of Figure 8 illustrates that, in some applications, it may be desirable to further synchronize a data operation with a recovered clock for the corresponding outgoing serial data. Figure 8 also shows that delay locked loop (DLL) circuits may be used in place of CDR circuits for particular applications.

[0060] One application of each of the above described embodiments is that of a protocol translator. specifically, referring to the embodiment of Figure 8, an integrated circuit may include a clock recovery circuitry coupled to receive a high data rate input data stream for recovering a clock, based on the high data rate input data stream. While the high data rate input serial data stream is received according to a first protocol, the selectable clock based functionality translates the input serial data stream from the first protocol to a second protocol at a selected recovered clock rate of the input serial data stream. As the second protocol serial data stream is produced, its transmission rate may be one that corresponds to the recovered clock rate from the input serial data stream or a different rate based upon translation performance factors. Accordingly, the outgoing serial data stream may be transmitted at a TX clock rate or even at a rate that corresponds with a translation rate.

[0061] Figure 9 is illustrates a block diagram of a clock and/or data recovery circuit 202 in accordance with one

embodiment of the present invention. The clock recovery circuit 202 includes a phase detector 204, a charge pump 206, a loop filter 208, a controlled oscillation module 210, and a feedback module 212.

Clock recovery circuit 202 receives a serial data stream 52, which may be a high data rate bit stream transferring data at 10 or more gigabits per second. detector 204 produces phase information 214 and error adjustment signal 216 based on the input serial data 52 and a feedback clock signal 224 (recovered clock). Operation of phase detector 204 is generally known by one of average skill in the art. Phase detector 204 produces phase information 214 to a charge pump such as charge pump 206. Charge pump 206 produces an error adjustment signal 216 based on the phase information 214. A loop filter 208 then produces an error signal 218 (a voltage signal) to an oscillation module 210. The controlled oscillation module 210 receives the error signal 218 and produces therefrom an oscillating signal 220. Feedback module 212 and divider 222 generate the feedback signal, which is the recovered clock signal 224, by dividing oscillating signal 220 by a divider value (could be "1", i.e., no division), and by converting the resulting oscillation to a digital signal to represent the recovered clock signal 224.

[0063] Figure 10 illustrates a schematic block diagram of receiver clock data recovery block 226 of a transceiver according to one embodiment of the present invention. The clock data recovery block 226 includes a coarse PLL and a fine PLL. In general, the coarse PLL establishes the desired frequency for the clocking circuit and the fine PLL adjusts the phase of the clock and it will also adjust a limited frequency offset to align it with the incoming data. In the present embodiment of the invention, the feedback signal frequency provided by feedback module 212 is one-half the frequency of the inbound serial data 52. The coarse PLL includes a crystal oscillator 228 (including, if necessary,

a clock multiplier), a coarse phase and frequency detector 230, a coarse charge pump 232, a buffer 234, and a coarse divider 236. The fine PLL, comprising clock recovery module 10 was described with reference to Figure 9.

To establish the operating frequency for the clocking circuit, crystal oscillator 228 produces a reference clock 238 that is provided to the coarse phase and frequency detector 230. The coarse phase and frequency detector 230 determines the phase and frequency difference between the reference clock 238 and a divided representation of receiver clock 240. The coarse divider 236 provides the divided representation of the receiver clock 240 to the coarse phase and frequency detector 230 as a feedback signal. Based on the phase and frequency relationship of these signals, coarse phase and frequency detector 230 produces a coarse difference signal 242. Coarse charge pump 232 receives the coarse difference signal 242 and produces a current representation (which is converted to voltage through the transimpedance included at the output of the fine PLL charge pump 206 thereof and provides a coarse error signal 244 to controlled oscillation module 210 of the fine loop filter 208. Controlled oscillation module 210 receives the coarse error signal 244, and adjusts the oscillation frequency of receiver clock 240. Once the coarse PLL has established the operating frequency, the fine PLL becomes active and adjusts the phase of the receiver clock.

[0065] Controlled oscillation module 210 may utilize inductor-capacitor oscillators or ring oscillators to produce an output oscillation. If a inductor-capacitor oscillator is utilized, noise levels of controlled oscillation module 208 may be reduced.

[0066] As illustrated, clock data recovery block 226 includes two phase locked loops. One is a fine phase locked loop based on the inbound serial data 52 and the other is a coarse phase locked loop based on reference clock 238. Such a sequential phased locked loop system enables the receiver

section to readily capture the inbound serial data 52. As one of average skill in the art will appreciate, clock data recovery block 226 may use single-ended signals or differential signals.

[0067] A plurality of methods of processing high data rate serial data utilizing the various embodiments of the transceivers illustrated in Figures 5-8 are illustrated in Figures 11-14. More specifically, Figure 11 illustrates a method for processing high data rate serial data according to a first embodiment of the invention. Initially, the method includes receiving a high data rate input data stream at the transceiver (step 250) and recovering a clock based on the high data rate input data stream (step 252). Thereafter, the transceiver method includes providing the recovered clock to an FPGA (or other programmable logic) fabric portion (step 254) and performing subsequent processing in the FPGA portion based on the recovered clock (step 256).

[0068] One embodiment of the inventive method further includes receiving the high data rate input data stream according to a first protocol and converting the high data rate input data stream to a second protocol based on the recovered clock (step 258). Once the data stream is converted to a second protocol, it is then transmitted (step 260). The data may be transmitted based on the first recovered clock, a second recovered clock (for example, recovered from a transmitter clock) or any other clock, such as a reference clock.

[0069] Figure 12 illustrates a method of processing high data rate serial data according to a second embodiment of the invention. The method initially includes receiving a first serial bit stream and recovering a clock from the first serial bit stream (step 262). Thereafter, the invention includes receiving a second serial bit stream and recovering a clock from the second serial bit stream (step 264). The transceiver of the present invention then

provides the first and second recovered clocks and a reference clock to a circuit portion (step 266). Finally, the method includes, within the circuit portion, choosing among the first and second recovered clocks and the reference clock for subsequent processing for a specified functionality (step 268). As previously described, the circuit portion may be a fixed circuit or may be programmable logic fabric.

Figure 13 illustrates a method of clock management [0070] according to a third embodiment of the invention. management in a processing block of a transceiver device includes receiving a first data stream and recovering a first clock based on the first data stream (step 270) and providing the first recovered clock to a first circuit portion (step 272). Additionally, the transceiver may receive a second data stream and recover a second clock based on the second data stream (step 274), and may provide the second recovered clock to a second circuit portion (step 276). The transceiver may also provide a reference clock to a third circuit portion (step 278). Finally, the processing block may concurrently perform processing functions in using one or more of the first and second recovered clocks and the reference clock (step 280).

[0071] Figure 14 illustrates a method of receiving and transmitting data high data rate serial data according to a fourth embodiment of the invention. Initially, the transceiver may receive a plurality of input data streams (step 282) and recover a corresponding plurality of clocks based on the plurality of input data streams (step 284). The transceiver may then determine at least one output port for providing outgoing data streams (step 286). The transceiver may then provide each input data stream to the at least one output port based upon a corresponding recovered clock (step 288). The method of providing the outgoing data streams to the at least one output port comprises, in one embodiment of the invention, providing the

outgoing data streams to a number of output ports that corresponds to a number of input data streams wherein the method further includes determining, for each input data stream, an output port and providing the input data streams to the determined output ports at a corresponding recovered clock of the corresponding plurality of recovered clocks (step 290).

[0072] The invention disclosed herein is adaptable to various modifications and alternative forms. Therefore, specific embodiments have been shown by way of example in the drawings and detailed description. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the invention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the claims.